

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In application of: RAMINDA U. MADURawe  
Application No.:  
Title: PROGRAMMABLE STRUCTURED ARRAYS  
Filed: 12/01/2003

INFORMATION DISCLOSURE STATEMENT SUBMISSION

Sirs:

Attached is IDS form 1449 along with copies of the references for the Application submitted herewith entitled "PROGRAMMABLE STRUCTURED ARRAYS".

Regards,

  
\_\_\_\_\_  
Raminda U. Madurawe


CERTIFICATE OF MAILING

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PTO/SB/08B (08-00)

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		Application Number	
		Filing Date	12/01/2003
		First Named Inventor	Madurawe, Raminda U.
		Group Art Unit	
		Examiner Name	
		Attorney Docket Number	
Sheet	2	of	2

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Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		SEALS & WHAPSHOTT, "Programmable Logic – PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA	<input type="checkbox"/>
		ASHOK K. SHARMA, "Programmable Logic Handbook – PLDs, CPLDs, & FPGAs", 1998, pp 99-171, McGraw-Hill, USA	<input type="checkbox"/>
		V. BETZ, J. ROSE, A. MARQUARDT, "Architecture and CAD for Deep-Submicron FPGAs", Feb 1999, Kluwer Academic Publishers, Boston	<input type="checkbox"/>
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